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SCULLY SCOTT MURPHY & PRESSER, PC
400 GARDEN CITY PLAZA
SUITE 300
GARDEN CITY, NY 11530

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JOHNSON, BRIAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,671	NAKAJIMA, HIROYUKI	
	Examiner	Art Unit	
	Brian P. Johnson	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-12 and 21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-12 and 21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 1, 3-12 and 21-40 have been examined.

Acknowledgment of papers filed: election and claims filed on 20 November 2006. The papers filed have been placed on record.

Claim Objections

2. Claim 27 and 28 are objected to because of the following informalities:

it appears Applicant intended to state "pipeline stage" rather than simply the word "pipeline".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Hammond (U.S. Patent No. 5,774,686).

5. Regarding claim 9, Hammond discloses a processor having a pipeline control architecture (Hammond fig. 8), said processor comprising: a unit for receiving a stage-number setting instruction; and a unit for setting variably the number of stages in the

pipeline control in response to the received stage-number setting instruction (Hammond col 15 line 47-53).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3-4, 6-8, 21-37, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond (U.S. Patent No. 5,774,686) in view of Trivedi (U.S. Patent No. U.S. Patent No. 6,430,674).

8. Regarding claim 1, Hammond discloses a processor having a plurality of processor functions for executing each of a plurality of instruction sets (col 4 lines 12-15), comprising: a system instruction decoder (fig. 8 reference 830 and 835) for decoding a system instruction that is not executed by any of the plurality of processor functions (col 14 line 48 to col 15 line 5); and a system instruction execution unit for selecting one of the plurality of processor functions in response to said system instruction decoded by said system instruction decoder (fig. 8 reference 840).

Hammond fails to disclose a decoder used exclusively for the switch instruction.

Trivedi discloses a decoder (fig. 3 reference 306) used only for the switch instruction (col 4 lines 23-27).

Hammond would have been motivated to utilize the detector to pick switch instructions out of a general decoder to save in area and power. Using shared logic for both decoders of Hammond would reduce the area of the design. Additionally, the detector is implimented to save power (col 6 line 47 to col 7 line 7).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hammond and allow a detector unit of Trivedi to detect switch instructions and decode them seerately from the rest of the instructions.

9. Regarding claim 3, Hammond/Trivedi discloses the processor according to claim 1, wherein at least two of the plurality of processor functions share hardware resources (Hammond fig. 8 reference 840 and col 15 lines 51-57).

10. Regarding claim 4, Hammond/Trivedi discloses the processor according to claim 1, wherein at least two of the plurality of instruction sets include a common instruction (Hammond col 15 line 47 to col 15 line 5),

Note that the switch instruction is considered to be the "common instruction"; however, the instruction sets have many common instructions that are only translated versions of the other (Hammond col 15 lines 47-53).

And a plurality of processor functions corresponding to said at least two instruction sets share an instruction set decoder for decoding the common instruction (Trivedi fig. 3 reference 306).

11. Regarding claim 6, Hammond/Trivedi discloses the processor according to claim 1, further comprising a storage unit for storing processing control data corresponding to each instruction included in the plurality of instruction sets (Hammond fig. 8 references 752 -758);

Note: In addition to the registers shown, a processor must contain many control signals to affect the performance of the execution unit, multiplexers and various other alterable modules within the processing system.

Wherein on the basis of an entered instruction and information regarding a selected processor function, an address that corresponds to the entered instruction is generated and processing control data corresponding to the entered instruction is read out of said storage unit (fig. 8 reference 734).

Note that the claim language is rather ambiguous. It sounds like it requires only an address being fetched (like from the cache) and the control signals of the instruction at that address being stored.

12. Regarding claim 7, Hammond/Trivedi discloses the processor according to claim 1, wherein at least two processor functions among the plurality thereof have a common instruction set (Hammond col 15 line 47 to col 15 line 5).

Note: see claim 4.

13. Regarding claim 8, Hammond/Trivedi discloses the processor according to claim 1, wherein at least one processor function among the plurality thereof undergoes

pipeline control in which number of stages thereof is set variably, and the number of stages in the pipeline control is set in response to a predetermined system instruction (Hammond col 15 lines 47-53).

Note that, for a particular instruction set, a separate decoding (translating) stage is added.

14. Regarding claim 21, Hammond/Trivedi discloses a processor apparatus comprising: an instruction fetch register for storing an instruction fetched (Hammond fig. 8 reference 732); a plurality of instruction decoders (Hammond fig. 8 references 830 and 835), each receiving and decoding an instruction of an instruction set associated with said instruction decoder (Hammond col 14 line 47 to col 15 line 5); a plurality of instruction execution controllers (Hammond fig. 8),

Note that little patentable weight is given to the distinction of a "plurality" of instruction controllers since, in any processing system, a single controller can be conceptually broken into several modules, each reasonably considered a separate controller.

Each being provided in association with the corresponding instruction decoder, for receiving a decoded result of the instruction by the corresponding instruction decoder for controlling the execution of the instruction;

Note that one purpose of a decoder is to generate control signals. The controller to which these signals are sent are considered to be associated to the controllers.

An instruction set change over unit for selecting at least one among the plurality of instruction decoders and for supplying an instruction output from said instruction fetch register to the selected instruction decoder (Hammond fig. 8 reference 820); a system instruction decoder receiving a predetermined system instruction from instruction fetch register for decoding the predetermined system instruction (Trivedi fig. 3 reference 306); and a system instruction execution controller receiving the decoded result from said system instruction decoder (Hammond fig. 8 reference 840); said system instruction execution controller controlling said instruction set change over unit to change over the selection of the plurality of instruction decoders, in accordance with said system instruction decoded by said system instruction decoder, in case said system instruction being an instruction specifying the instruction set to be used among a plurality of instruction sets (Trivedi col 4 lines 24-27 and Hammond col 15 line 47 to col 15 line 5).

15. Regarding claim 22, Hammond/Trivedi discloses the processor apparatus according to claim 21, wherein said system instruction execution controller performs control to dynamically change over the number of stages in a pipeline from an instruction fetch stage to an instruction execution stage for an instruction set being used, in accordance with said system instruction decoded by said system instruction decoder, in case said system instruction being an instruction that specifies the number of pipeline stages for the instruction set (Hammond col 15 lines 47-53).

Note: see claim 8.

16. Regarding claim 23, Hammond/Trivedi discloses the processor that performs a first instruction set and a second instruction set and a second instruction set, comprising:

a first processing unit that executes processing based on only a first decoded result, among a first decoded result and a second decoded result, the first decoded result being a decoded signal of an instruction included in the first instruction set, the second decoded result being a decoded signal of an instruction included in the second instruction set (Hammond fig. 8 reference 850 and 855; col 14 lines 14-16); and

a common processor unit that executes processing based on both the first and second decoded results (Hammond fig. 8 reference 840).

17. Regarding claim 24, Hammond/Trivedi discloses the processor according to claim 23, further comprising:

a first decoder that generates the first decoded result by decoding the instruction included in the first instruction set (Hammond fig. 8 reference 830); and

a second decoder that generates the second decoded result by decoding the instruction included in the second instruction set (Hammond fig. 8 reference 835).\

18. Regarding claim 25, Hammond/Trivedi discloses the processor according to claim 24, further comprising:

a second processing unit that executes procession based on only the second decoded result among the first and second decoded results (Hammond fig. 8 reference 855)

19. Regarding claim 26, Hammond/Trivedi discloses the processor of claim 23, further comprising:

a common instruction set decoder that decodes a common instruction including commonly in the first and second instruction sets (Trivedi fig. 3 reference 306).

20. Regarding claim 27, Hammond/Trivedi discloses the processor of claim 24, further comprising:

a pipeline stage that is provided between the first decoder and the first processing unit (Hammond fig. 8 references 825, 740 and 840).

21. Regarding claim 28, Hammond/Trivedi discloses the processor of claim 25, further comprising:

a first pipeline provided between the decoder and the first processing unit; and a second pipeline provided between the second decoder and the second processing unit (Hammond fig. 8 references 825, 740, and 840).

22. Regarding claim 29, Hammond/Trivedi discloses the processor of claim 28, wherein the first pipeline stage has a different number from said second pipeline (Hammond col 15 lines 47-53).

23. Regarding claim 30, Hammond/Trivedi discloses the processor of claim 27, wherein said stage number of the pipeline is variable (Hammond col 15 lines 47-53).

24. Regarding claim 31, Hammond/Trivedi discloses the processor of claim 28, wherein the stage number of the first and second pipeline are variable (Hammond col 15 lines 47-53).

25. Regarding claim 32, Hammond/Trivedi discloses the processor of claim 24,further comprising a system instruction decoder that decodes a system instruction which selects use of any one of the first and second decoders (Hammond col 14 line 48 to col 15 line 5 and Trivedi fig. 3 reference 306).

26. Regarding claim 33, Hammond/Trivedi discloses the processor of claim 32, wherein said system instruction decoder is provided separate from the first and second decoders (Trivedi fig. 3 reference 306).

27. Regarding claim 34, Hammond/Trivedi discloses the processor of claim 24, wherein any one of the first and second decoders is selected for use in response to an interrupt signal (Hammond col 14 line 48 to col 15 line 5).

28. Regarding claim 35, Hammond/Trivedi discloses the processor of claim 32, wherein said system instruction includes at least one of instructions for setting power voltage and/or operating rate at which the processor operates (Trivedi col 7 lines 4-7).

29. Regarding claim 36, Hammond/Trivedi discloses the processor according to claim 23, further comprising:

a memory that stores both the first and second decoded results (Hammond fig. 8 references 850 and 855, as a single entity).

30. Regarding claim 37, Hammond/Trivedi discloses the processor according to claim 36, further comprising:

a second processing unit that executes processing based only on the second decoded result among the first and second decoded results (Hammond fig. 8 reference 855).

31. Regarding claim 40, Hammond/Trivedi discloses the processor according to claim 23, further comprising: a register file being specific to the first instruction set (col 14 lines 14-16).

Note that the fact that instructions can access information from a different instruction sets' register file doesn't mean that the register files aren't specific to a particular register file. The register files are still organized to complete instructions of a particular instruction set and have memory allotments that are specific to the instruction set.

32. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond/Trivedi in view of Dalvi (U.S. Patent No. 6,167,529).

33. Regarding claim 5, Hammond/Trivedi discloses an instruction that sets the power-supply voltage at which the processor operates (Trivedi col 7 lines 5-8).

Hammond/Trivedi fails to disclose an instruction that alters the clock frequency.

Dalvi discloses switching the operating speed based on the instruction to be executed (col 2 lines 40-51).

Hammond/Trivedi would have been motivated to utilize the teachings of Dalvi because it allows each architecture to be executed at it's greatest potential with respect to power and speed.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the computing system of Hammond/Trivedi and allow the switch instruction (causing a change in instruction set) to set the speed of the processor, similar to the teachings of Dalvi.

34. Claims 10, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond/Trivedi in view of Glass (U.S. Patent No. 5,774,686).

35. Regarding claim 10, Hammond discloses the processor of claim 1.

Hammond fails to disclose that it is on an integrated circuit.

Glass discloses a system on an integrated circuit (col 4 lines 21-25).

At the time of the invention, one skilled in the art would have been motivation to make the combination based on the reasoning disclosed in Glass that an integrated circuit "is highly advantageous for space, speed, power consumption and cost reasons" (col 4 lines 23-25).

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hammond and integrate it in an IC as disclosed in Glass.

36. Regarding claim 11, Hammond/Trivedi/Glass discloses a system LSI circuit having a plurality of the processors set forth in claim 1.

Examiner takes Official Notice that it is commonly known in the art that multi-processing systems can dramatically increase throughput. Hammond/Glass would have been motivated to utilize a multi-processing system for that reason.

37. Regarding claim 12, Hammond/Glass discloses the system LSI circuit according to claim 11, wherein the plurality of processors operate based upon either a first pattern in which all processors operate according to the same instruction set, or a second

pattern in which at least one processor operates according to an instruction set that is different from those of the other processors.

Note that the references, as combined, create instruction set options that are entirely user controlled. For that reason, the processor has the option to do each of the modes described in this claim, based on the positioning of the switching instructions.

38. Claim 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond/Trivedi in view of Kahle (U.S. Patent No. 6,725,354).

39. Regarding claim 38, Hammond/Trivedi discloses a processor that performs a first instruction nset and a second instruction set, comprising: a first processing unit that executes processing based on only a first decoded result, among the first decoded result and a second decoded result (col 15 lines 34-46), the first decoded result being a decoded signal of an instruction included in the first instruction set, the second decoded result being a decoded signal of an instruction included in the second instruction set (col 15 lines 34-46)

Hammond/Trivedi fails to disclose a common processor unit based on the interpretation of this claim.

Kahle discloses two instruction paths having a shared execution unit for common instructions (col 1 lines 32-62).

Hammond/Trivedi would have been motivated to utilize this technique to increase efficiency of the system by increasing parallelization but limiting the amount of hardware available.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Hammond/Trivedi and include a common execution unit of Kahle. The combination would follow the pattern provided in Hammond col 15 lines 34-46 where each execution unit contains its own register file, which satisfies the limitations of claim 38.

40. Regarding claim 39, Hammond/Trivedi/Kahle discloses the processor according to claim 37, further comprising: a first register file for the first processing unit (fig. 8 reference 850; col 15 lines 34-46), a second register file for the second processing unit (fig. 8 reference 855; col 15 lines 34-46), and a common register file for the common processor unit (Kahle col 1 lines 32-62; Hammond col 15 lines 34-46).

Response to Arguments

41. Applicant's arguments filed 21 May 2007 have been fully considered but they are not persuasive.

42. Applicant states:

"Hammond discloses a fixed procedure, not a variable number of stages. Because the procedure of Hammond is fixed, Hammond does not disclose or suggest setting variably the number of stages in a pipeline control architecture in response to the received stage-number setting instruction, as recited in claim 9. Thus, Hammond does not disclose or suggest each feature of claim 9."

Applicant further states:

"Hammond does not disclose either stage-number setting instructions or setting variably the number of stages in a pipeline control architecture and hence does not disclose each and every feature of the invention has recited in independent claim 9, so that it is patentable over the art of record in the application."

Examiner disagrees. Col 15 lines 47-53 discloses an embodiment of the invention with a translator that translates x86 based instructions into a 64-bit based instruction set. This is different than the embodiment shown in fig. 8 where both decoders are in parallel. In the citation, an embodiment is described where translator 830 is connected serially to decoder 835. This means that x86 instructions will require an extra pipeline stage than 64-bit instructions (that will bypass the translator and go immediately to decoder 835). Consequently, an x86 instruction can be considered a "stage-number setting instruction" where the number of stages are variably set in response to receiving said stage-number setting instruction.

43. Applicant states:

"The Examiner asserts that Trivedi discloses a decoder used exclusively for the switch instruction. Applicant respectfully disagrees. Trivedi discloses a detector that can detect the presence of a mode switch instruction in the decoder (column 4, lines 24-26). Trivedi further discloses multiple decoders, one for each instruction set (column 4, liens 2-24). The multiple decoders of Trivedi decode instructions into fixed length microcode that are then executed (column 4, lines 28-31, emphasis added). However, Trivedi does not disclose or suggest 'a system instruction decoder, provided separately of the plurality of processor functions, for decoding a system instruction not executed by any of the plurality of processor functions' as recited in claim 1."

Examiner disagrees. Col. 1 initially describes "a plurality of processor functions for executing each of a plurality of instruction sets." Examiner considers these processor functions to be execution units 304 (see also col 4 lines 4-20) excluding the particular execution unit that governs the switch instruction. It follows that Trivedi

discloses "a system instruction decoder (*detector 306*), provided separately of the plurality of processor functions (*in particular, separately from the execution units 304 that do not execute the switch instruction*), for decoding a system instruction not executed by any of the plurality of processor functions (*again, the "plurality of processor functions" do not execute the switch instruction*).

44. Applicant states:

"Regarding independent claim 21, as discussed above, Trivedi discloses a decoder 302b and a detector 306 which can detect the presence of a mode switch instruction in the decoder. Trivedi does not disclose or suggest a system instruction decoder receiving a predetermined system instruction. Thus, the hypothetical combination of Hammond and Trivedi does not disclose or suggest each feature of independent claim 21."

It is unclear where the confusion lies with this rejection. Perhaps Applicant does not believe that a detector can be properly used to anticipate a decoder. If this is the case, Examiner disagrees. A decoder is a module within a microprocessor that receives instruction bits and generates appropriate control signals based on the instruction type. This is clearly the functionality of the detector (fig. 3; col 6 lines 47-55).

45. Applicant states:

"Further, the Examiner asserts that Hammond discloses a first processing unit that executes processing based on only a first decoded result among a first decoded result and a second decoded result, and a common processor unit that executes processing based on the first and second decoded results, as recited in independent claim 23. Applicant respectfully disagrees. Hammond discloses an execution unit 840 to execute the decoded instructions from both instruction sets (column 14, lines 11-14). No other processing units are disclosed. Further, Hammond discloses that the register file 850 stores the values related to the x86 instruction set and is accessed by the execution unit 840 based on the instructions in the 64-bit instruction set, and therefore the register 850 does not execute processing based on only the decoded results of the x86 instruction set (column 14, lines 14-35, Figure 8)."

Examiner disagrees. Applicant's characterization of Hammond appears to be correct; however, Applicant's arguments appear to be based on limitations that do not

exist within claim 23. It is true if "a first decoded result" is an X86 instruction storing information in its corresponding register file and "a second decoded result" is a 64 bit instruction that accesses the X86 register file as described in col 14 lines 14-35, then it follows that the first processing unit would not execute processing based only on a first decoded result. Therefore, it is true that an embodiment of the reference can be found that does not anticipate claim 23.

However, this fact does not make the rejection improper. Examiner is required to find only one embodiment of the invention that anticipates the claim. Therefore, when "a first decoded result" as an X86 instruction storing information in its respective register and, similarly, "a second decoded result" is a 64-bit instruction storing information in its respective register file, the remaining limitations of the claim logically follow. The execution unit 840 processes based on both decoded results; the X86 register file processes based only on the first decoded result; and the 64 bit register file processes based only on the second decoded result. The claim is properly rejected.

46. Examiner further notes that claim 1 does not contain all the limitations of claim 2. In fact, the amendment requires "one of said system instruction decoded by said system instruction decoder, and a prescribed interrupt signal" as opposed to "said system instruction decoded by said system instruction decoder." Therefore, claim 1 is now more broad than it was initially since only "one of" the remaining limitations are required to be found in prior art.

Conclusion

47. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P. Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on 8-4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100